On page 47, line 5, delete "from left to right" and substitute -- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

151. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a write request to the memory device, wherein in response to the write request, the memory device samples first and second portions of data;

providing a first portion of data to the memory device synchronously with respect to a rising edge transition of an external clock signal; and

providing a second portion of data to the memory device synchronously with respect to a falling edge transition of the external clock signal.

152. The method of claim 151 wherein the write request, the first portion of data and the second portion of data are included in a packet.

153. The method of claim 151 wherein the write request, the first portion of data and the second portion of data are included in the same packet.

154. The method of claim 151 further including:

providing block size information to the memory device, wherein the block size information defines a first amount of data to be input by the memory device in response to a write request wherein:

a first portion of the first amount of data is sampled by the memory device in response to a rising edge transition of the external clock signal; and

a second portion of the first amount of data is sampled by the memory device in response to a falling edge transition of the external clock signal.

155. The method of claim 151 further including:

providing block size information to the memory device, wherein the block size information defines a first amount of data to be output by the memory device in response to a read request;

issuing a read request to the memory device; and

receiving the first amount of data from the memory device.

156. The method of claim 155 further including providing access time information to the memory device, wherein the access time information is representative of a number of clock cycles of the external clock signal to delay before the memory device outputs the first amount of data.

157. The method of claim 151 further including:

providing the external clock signal to the memory device wherein:

in response to a rising edge transition of the external clock signal the memory device samples the first portion of the data; and

in response to a falling edge transition of the external clock signal the memory device samples the second portion of the data.

158. A method of controlling a memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a write request to the memory device, wherein in response to the write request, the memory device samples first and second portions of data;

providing a first portion of data to the memory device synchronously with respect to a first external clock signal; and

providing a second portion of data to the memory device synchronously with respect to a second external clock signal.

159. ~~The method of claim 158 wherein the write request, the first portion of data and the second portion of data are included in a packet.~~

160. The method of claim 158 wherein the write request, the first portion of data and the second portion of data are included ~~in the same packet.~~

161. The method of claim 158 further including:

providing block size information to the memory device, wherein the block size information defines a first amount of data to be input by the memory device in response to a write request; and

wherein a first portion of the first amount of data is sampled synchronously with respect to the first external clock signal, and a second portion of the first amount of data is sampled synchronously with respect to the second external clock signal.

162. The method of claim 158 further including:

providing block size information to the memory device, wherein the block size information defines a first amount of data to be output by the memory device in response to a read request; and

receiving the first amount of data from the memory device.

163. The method of claim 162 further including:

providing access time information to the memory device, wherein the access time information is representative of a number

of clock cycles of the first external clock signal to delay before the memory device outputs data.

164. The method of claim 158 further including:

providing the first and second external clock signals to the memory device, wherein:

the first portion of data is sampled by the memory device synchronously with respect to the first external clock signal; and

the second portion of data is sampled by the memory device synchronously with respect to the second external clock signal.

165. The method of claim 164 wherein the first and second external clock signals are small voltage swing signals.

166. A memory controller for controlling a synchronous memory device, the memory controller comprising:

output driver circuitry to output data wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of a first external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the first external clock signal.

167. The memory controller of claim 166 further including: multiplexer circuitry coupled to the output driver circuitry, wherein:

in response to the first transition of the external clock signal, the multiplexer circuitry couples the first portion of data to an input of the output driver circuitry; and

in response to the second transition of the external clock signal, the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry.

168. The memory controller of claim 167 further including a delay lock loop circuit coupled to the external clock signal, the delay lock loop circuit generating a first internal clock signal, wherein the multiplexer circuitry couples the first portion of data to ~~the input of~~ the output driver circuitry in response to the first internal clock signal.

169. The memory controller of claim 168 wherein the delay lock loop circuit generates a second internal clock signal, wherein the multiplexer circuitry couples the second portion of data to the ~~input of the~~ output driver circuitry in response to the second internal clock signal.

170. The memory controller of claim 166 wherein both the rising edge transition of the first external clock signal and the

falling edge transition of the external clock signal transpire in one clock cycle of the first external clock signal.

171. The memory controller of claim 166 wherein both the rising and falling edge transitions of the first external clock signal include voltage swings of less than one volt.

172. A memory controller for controlling a synchronous memory device, the memory controller comprising:

output driver circuitry to output data wherein:

the output driver circuitry outputs a first portion of data in response to a first external clock signal; and

the output driver circuitry outputs a second portion of data in response to a second external clock signal.

173. The memory controller of claim 172, further including:

multiplexer circuitry coupled to the output driver circuitry, wherein:

in response to the first external clock signal, the multiplexer circuitry couples the first portion of data to an input of the output driver circuitry; and

in response to the second external clock signal, the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry.